KP628MD

USB Dedicated Charging Port Controller For Fast Charging Protocol

Description

The KP628MD is a fast charging protocol controller for HI Silicon Fast Charging Protocol (FCP) and Qualcomm® Quick Charge™ 2.0/3.0 (QC 2.0/3.0) USB interface. The KP628MD monitors USB D+/D− data line and automatically adjusts the output voltage depending on different powered device (PD). The charging time of PD is therefore optimized by the KP628MD.

KP628MD can support not only USB BC compliant devices, but also Apple / Samsung / HUAWEI devices and automatically detects whether a connected powered device is QC 2.0/3.0 or FCP capable before enabling output voltage adjustment. If a PD is not compliant with QC 2.0/3.0 and FCP, the KP628MD will disable the adjustment of output voltage and keep the default 5V output voltage for safe operation.

The KP628MD is available in a space-saving SOT-23-6 package.

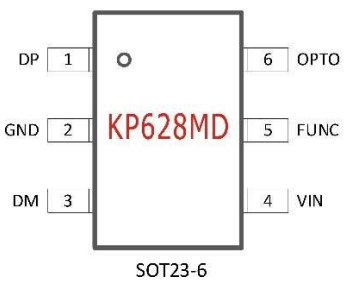
Features

- Supports Hi Silicon Fast Charging Protocol (FCP)
- Supports Qualcomm® Quick ChargeTM 2.0/3.0 Class A : 3.6V up to 12V Output Voltage
- Automatically Selects FCP and QC2.0/3.0 Protocols
- Supports USB DCP Shorting D+ Line to D− Line per USB Battery Charging Specification, Revision 1.2
- Complies with Chinese Telecommunication Industry Standard YD/T 1591-2009
- Suppors USB DCP Applying 2.7V on D+ Line and 2.7V on D− Line
- SOT-23-6 Package

Applications

- Wall-Adapter, Smart Phones, Tablets, Notebooks
- Mobile/ Tablet Power Bank
- Car Charger
- USB Power Output Ports

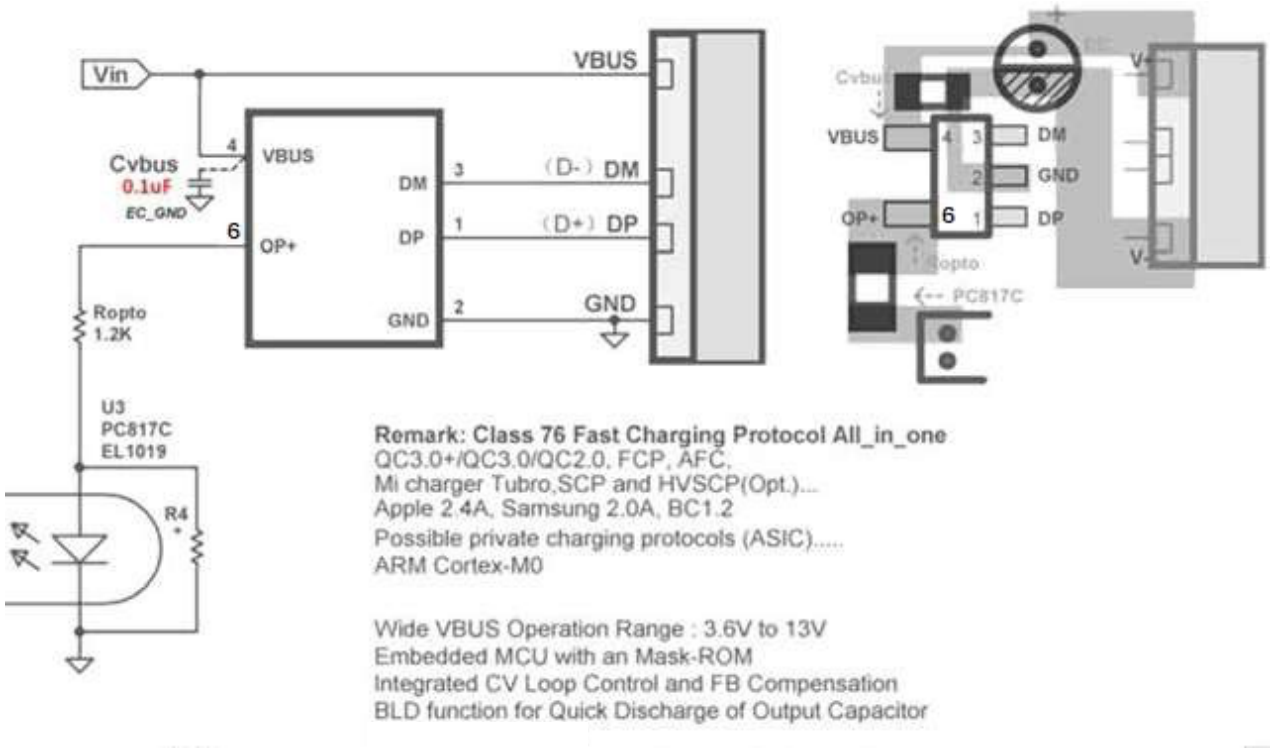
Pin Configurations



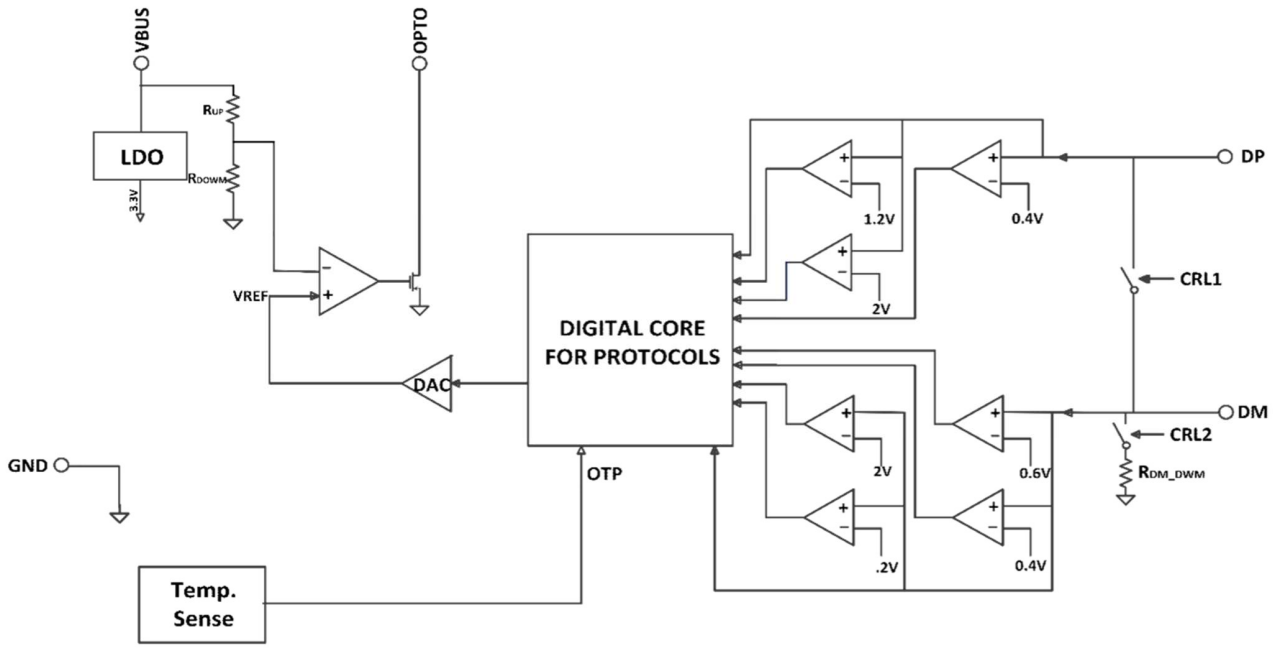
SOT23-6

PIN NO.	PIN NAME	FUNCTIONS
1	DP	USB DP, Connect to DP end of USBA.
2	GND	GND
3	DM	USB DM, Connect to DP end of USBA.
4	VIN	Power supply terminal of chip
5	FUNC	Floating
6	OPTO	Feedback control, Connected to the optical coupler through a resistor of 1KR

Typical Application Circuit



Function Block diagram



Ordering Information

Package	Part Number		Marking ID		Packing Type
	Pb-free	Halogen-free	Pb-free	Halogen-free	
SOT23-6	KP628MD	KP628MD	KP628MD	KP628MD	Reel & Carton

Absolute Maximum Ratings

(NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device)

Parameter	Min.	Max.	Unit
Vbus voltage range	-0.3	12	V
DP/DM voltage range	-0.3	15	V
OPTO voltage range	-0.3	5	V
The voltage range of others pin	-0.3	5	V
Operating junction temperature TJ	-20	150	℃
Leading Temperature (10s)	---	260	℃
ESD, CDM model per JEDEC EIA/JESD22-C101F	---	1000	V
Latch-up test per JEDEC 78	---	200	V
ESD, HBM model per Mil-Std-883H, Method 3015	---	2000	V
ESD, MM model per JEDEC EIA/JESD22-A115	---	200	V

Electrical Characteristics

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power						
VDD Input Voltage Range	V_{DD}		3.2		6.8	V
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{DD} Falling	2.5		2.9	V
VDD Supply Current		V_{DD} =5V, Measure V_{DD}		180		μA
VDD Shunt Voltage	$V_{DD(SHUNT)}$	IV_{DD} = 3mA	5.9	6.4	6.8	V
High Voltage Dedicated Charging Port (HVDCP)						
Data Detect Voltage	$V_{DAT(REF)}$		0.25	0.325	0.4	V
Output Voltage Selection Reference	V_{SEL_REF}		1.8	2.0	2.2	V
D+ High Glitch Filter Time	$T_{GLITCH(BC)-D+\_H}$		1000	1250	1500	ms
D− Low Glitch Filter Time	$T_{GLITCH(BC)-D-\_L}$			1		ms
Output Voltage Glitch Filter Time	$T_{GLITCH(V)CHANGE}$		20	40	60	ms
D− Pull-Down Resistance	$R_{D-(DWN)}$			20		kΩ
Continuous Mode Glitch Filter Time (Note 4)	$T_{GLITCH-CONT-CHANGE}$		100		200	μs
D+ Leakage Resistance	$R_{DAT-LKG}$	V_{DD} =3.2-6.4V,VD+=0.6-3.6V Switch SW1=Off	300	500	800	kΩ
Switch SW1 On-Resistance	$R_{DS\_ON\_N1}$	V_{DD} =5V,SW1= 200μA			40	Ω
Up/Down Current Step	I_{UP}, I_{DOWN}	I_{UP} = 40μA (9V), 70μA (12V), I_{DOWN} = 14μA (3.6V)		2		μA
Feedback Output Voltage	V_{FBO}		0.4		1.5	V
DCP Charging Mode						
$D+_{\_0.48V}$/$D-_{\_0.48V}$ Line Output Voltage			0.44	0.48	0.52	V
$D+_{\_0.48V}$/$D-_{\_0.48V}$ Line Output Impedance				900		kΩ

(VDD=5V, T_A=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Apple Mode						
$D+_{\_2.7V}/D-_{\_2.7V}$ Line Output Voltage			2.57	2.7	2.84	V
$D+_{\_2.7V}/D-_{\_2.7V}$ Line Output Impedance				33.6		kΩ
D- SECTION (FCP)						
D- FCP Tx Valid Output High	V_{TX-VOH}		2.55		3.6	V
D- FCP Tx Valid Output Low	V_{TX-VOL}				0.3	V
D- FCP Rx Valid Output High	V_{RX-VIH}		1.4		3.6	V
D- FCP Rx Valid Output Low	V_{RX-VIL}				1.0	V
D- Output Pull-Low Resistance (FCP) (Note 4)	R_{PD}		400	500	600	Ω
Unit Interval For FCP PHY Communication	UI	f_{CLK} = 125kHz	144	160	180	μs
Others						
QC_EN High-Level Input Voltage	V_{IH}		1.2			V
QC_EN Low-Level Input Voltage	V_{IL}				0.4	V

Note 4: Not production tested.

Typical Performance Curves

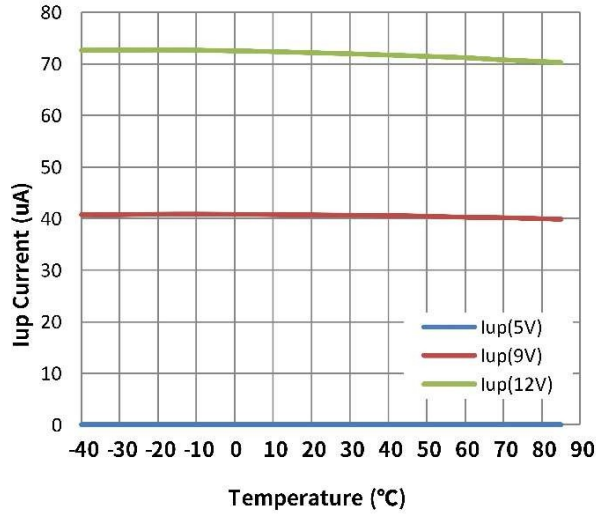


Figure4. UP Currentvs. Temperature

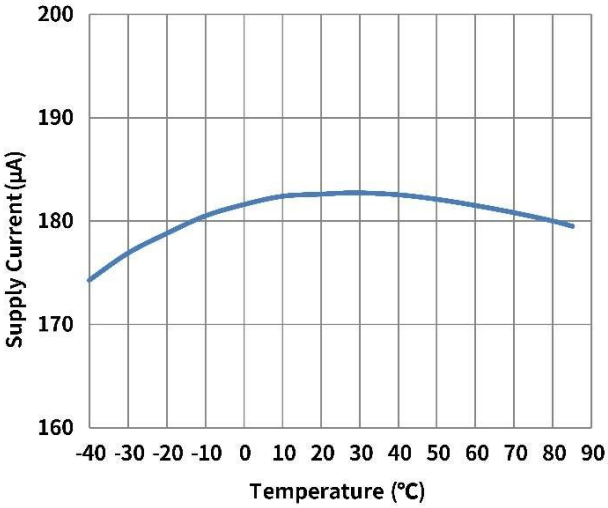


Figure5. SupplyCurrent vsTemperature

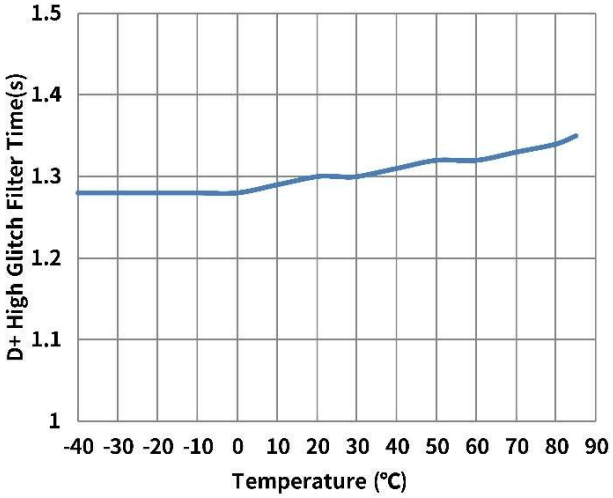


Figure6. D+ High Glitch Filter Time vs. Temperature

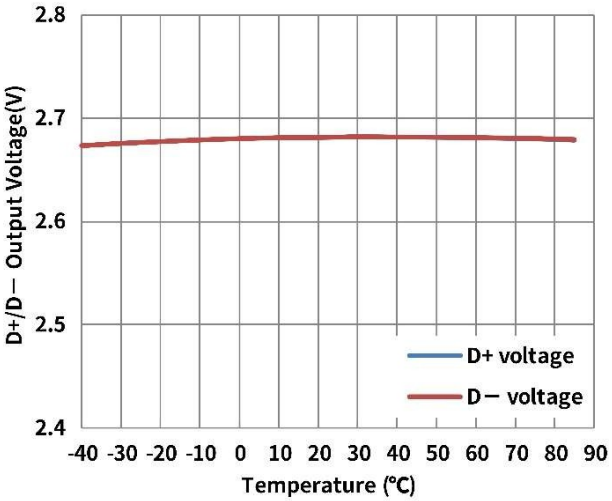


Figure7. D+/D- Output Voltage vs. Temperature

Application Information

Function Description

The KP628MD integrates both USB high voltage dedicated charging port interface IC for Qualcomm® Quick ChargeTM 2.0/3.0 class A and HI Silicon FCP specification.

The KP628MD can fast charge most of the handheld devices. It could be treated as the original charging adapter.

The KP628MD supports BC1.2, Samsung and HUAWEI devices. It also supports output voltage range of QC 3.0 Class A (3.6V to 12V) or QC 2.0 Class A (5V, 9V, 12V).

Quick Charge 2.0/3.0 Interface

When the KP628MD is powered on, D+ and D− pin are applied to 2.7V for Apple device. If handheld device has the function of QC 2.0/3.0, D+ pin will be forced between 0.325V and 2V. In the meanwhile, D+ pin will short to D− pin through the switch SW1 for entering BC 1.2. If D+

is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the KP628MD will enter QC 2.0/3.0 or FCP operation mode.

When the voltage of D+ pin and D− pin simultaneously satisfy these two inequalities VDAT(REF)< D+ <VSEL_REF and D− > VSEL_REF, the KP628MD would enter continuous mode.

In the continuous mode, each voltage pulse on D+ pin generated by powered device is between 1V and 3V. In the meanwhile, the high level of pulse should be kept at least 200us. If the specified conditions are satisfied, the FBO pin will sink 2uA per pulse. The maximum sink current is 70uA for output voltage 12V.

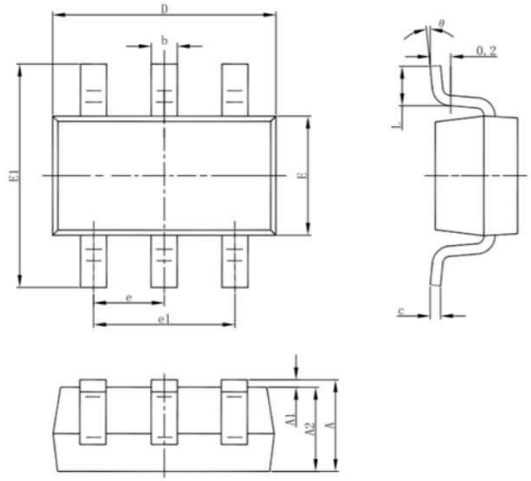
In the continuous mode, each voltage pulse on D− pin generated by powered device is between 3V and 1V. At the same time, the low level of pulse should be kept at least 200us. If the specified conditions are satisfied, the FBO pin will source 2uA per pulse. The maximum source current is 14uA for output voltage 3.6V.

If the powered device doesn't support QC 2.0, the KP628MD will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of D+ pin is therefore lower than VDAT(REF) and the output default voltage 5V is also applied.

Data Line Protection

When D+/D− pin is touched by the output voltage in abnormal situation, the D+/D− pin of both sink device and source device may be damaged. In order to protect the D+/D− pin of the devices from damage in abnormal situation, the KP628MD will return the output voltage to default output voltage 5V when the voltage of D+/D− pin is touched larger than 7.5V.

Package (SOT23-6)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°